CLAIMS

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1. A method for manufacturing an integrated semiconductor device, having a plurality of connection levels, comprising:

forming a first conductive region inside or above a substrate of semiconductor material;

forming a first insulating region of dielectric material above the first conductive region;

forming a first through region of electrically conductive material inside the first insulating region, and in direct electrical contact with the first conductive region;

forming a second conductive region above the first insulating region, in a position not aligned and not in contact with the first through region;

forming a second insulating region of dielectric material, covering the second conductive region;

forming, inside the second insulating region, a second through region of electrically conductive material, extending as far as the first through region, aligned and in direct electrical contact with the first through region; and

forming, above the second insulating region, a third conductive region aligned and in direct electrical contact with the second through region.

2. The method according to claim 1 wherein the first and second through regions have a substantially constant cross-sectional dimension.

3. The method according to claim 1 wherein the step of forming the first conductive regions comprises the step of introducing doping ion species inside the substrate.

4. The method according to claim 1 wherein the first conductive region is of metal material, a third insulating region extends above the substrate, and the first conductive region extends above the third insulating region.

5. The method according to claim 1 wherein the second and the third conductive regions are formed in successive metal levels.

6. The method according to claim 1 wherein the first insulating region comprises a first insulating layer of a first dielectric material, and a second insulating layer of a second dielectric material, superimposed on each other, the step of forming the first through region comprises, in succession, the steps of etching the second dielectric material with first etching parameters, etching the first dielectric material with second etching parameters, thereby forming a through aperture in the first insulating region, and filling the through aperture with the electrically conductive material.

7. The method according to claim 6 wherein the first dielectric material comprises silicon oxide, and the second dielectric material comprises silicon nitride.

8. A method according to claim 6 wherein the first dielectric material comprises silicon nitride, and the second dielectric material comprises silicon oxide.

9. A method of forming a semiconductor structure electrically coupling two conductive regions separated by at least two insulating layers, comprising:

forming a first conductive region;

forming a first insulating layer having an upper surface over the first conductive region;

etching a first opening through the first insulating layer to expose a portion of the first conductive region;

forming a first conductive plug that fills the first opening and is electrically coupled to the first conductive region, the first conductive plug having an upper surface extending no further than the upper surface of the first insulating layer;

forming a second insulating layer having an upper surface over the first insulating layer;

etching a second opening through the second insulating layer to expose a portion of the upper surface of the first conductive plug;

forming a second conductive plug that fill the second opening and is electrically coupled to the first conductive plug, the second conductive plug directly contacting the upper surface of the first conductive plug, and further having an upper surface extending no further than the upper surface of the second insulating layer; and

forming a second conductive region over the second insulating layer, the second conductive region being electrically coupled to the first conductive region through the first and second conductive plugs.

10. The method of claim 9 wherein forming the first conductive region comprises implanting a dopant into a substrate over which the first insulating layer is formed.

11. The method of claim 9 wherein forming the first conductive region comprises depositing a semiconductor material prior to forming the first insulating layer.

12. The method of claim 9 wherein forming the first conductive plug comprises:

depositing a conductive layer over the first insulating layer and filling the first opening; and

removing the conductive layer over the first insulating layer by polishing to leave conductive material filling the first contact via.

13. The method of claim 9 wherein forming the second insulating layer comprises:

forming a first dielectric layer over the first conductive region; and

forming a second dielectric layer over the first dielectric layer.

14. The method of claim 13 wherein forming the second opening comprises etching through the second dielectric layer and subsequently etching through the first dielectric layer.

15. A method for manufacturing an integrated semiconductor device, having a plurality of connection levels, comprising:

forming a first conductive region inside or above a substrate of semiconductor material;

forming a first insulating region on the first conductive region;

forming a first opening completely through the first insulating region, thereby exposing the first conductive region;

forming a first through region by filling the first opening with electrically conductive material to directly contact the first conductive region;

forming a second insulating region on the second conductive region and the first insulating region;

forming a second opening completely through the second insulating region, thereby exposing the first through region;

forming a second through region by filling the second opening with electrically conductive material to directly contact the first through region; and

forming, above the second insulating region, a second conductive region aligned and in direct contact with the second through region.

16. The method according to claim 15, further comprising forming a third insulating region on the substrate, wherein the first conductive region extends above the third insulating region.

17. The method according to claim 15 wherein the first and second conductive regions are formed in successive metal levels.

18. The method according to claim 15 wherein the first insulating region comprises a first insulating layer of a first dielectric material, and a second insulating layer of a second dielectric material, superimposed on each other, and the step of forming the first opening comprises selectively etching the second dielectric material with respect to the first dielectric material and then etching the first dielectric material.

19. The method according to claim 18 wherein the first dielectric material comprises silicon oxide, and the second dielectric material comprises silicon nitride.

20. A method according to claim 18 wherein the first dielectric material comprises silicon nitride, and the second dielectric material comprises silicon oxide.